KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

FOR MESSRS:_____ DATE : Oct. 8th ,2012

CUSTOMER'S ACCEPTANCE SPECIFICATIONS

TX38D18VM2BAA

Contents

ACCEPTED BY:_____ PROPOSED BY: Dan Chung

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 15” XGA of 4:3 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R (red), G (green), B (blue) sequentially. This display is RoHS compliant, COF (chip on film) technology and LED backlight are applied on this display.

Part Name	TX38D18VM2BAA
Module Dimensions	326.5(W) mm x 253.5(V) mm x 11.5 (D) mm
LCD Active Area	304.1(H) mm x 228.1(V) mm
Pixel Pitch	0.297(W) mm x 0.297 (H) mm
Resolution	1024 x 3(RGB)(W) x 768(H) dots
Color Pixel Arrangement	R, G, B Vertical stripe
LCD Type	Transmissive Color TFT; Normally White; Anti-Glare Polarizer
Display Type	Active Matrix
Number of Colors	16.7M / 262k Colors
Backlight	39 LEDs (13 series x 3)
Weight	(850g)
Interface	1ch - LVDS / Receiver; 20 pins
Power Supply Voltage	3.3V for LCD; 12V and 5V for Backlight
Power Consumption	(1.7W) for LCD; (13.2 W) for Backlight
Viewing Direction	12 O’clock (without image inversion and least brightness change)

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4	V	-
Input Voltage of Logic	V_I	-0.2	V_{DD}+0.3	V	Note 1
Operating Temperature	Top	-30	80	°C	Note 2
Storage Temperature	Tst	-30	80	°C	Note 2
Backlight Input Voltage	V_{LED}	10	30	V	-
Input Voltage of backlight control	V_{LEDC}	0	6.0	V	Note 3

Note 1: The rating is defined for the signal voltages of the interface such as DE, DCLK, FRC and pixel data signal.

Note 2: The maximum rating is defined as above based on the temperature on the panel surface and LED driver board, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25°C.
- Operating under high temperature will shorten LED lifetime.
- Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Note 3: The Backlight control signal voltage of the interface such as EN,DDIM and ADIM signal.

5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

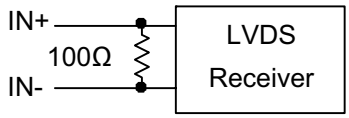
$T_a = 25\ ^{\circ}C,\ \mathrm{Vss} = 0\mathrm{V}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Ripple Voltage	V_{RP}	-	-	-	100	mVp-p	
Rush Current	I_{RUSH}	-	-	-	2.0	A	Note 1
Differential Input Voltage for LVDS Receiver Threshold	V_I	V_{IH}	-	-	+100	mV	Note 2
		V_{IL}	-100	-	-		
Power Supply Current	I_{DD}	White Pattern	-	410	510	mA	Note 3,4
		Black Pattern	-	590	690		
DCLK Frequency	f_{CLK}	-	-	65	80	MHz	-

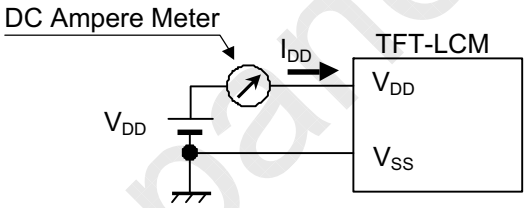
Note 1: Rush current is set maximum 2A. Current capacity for V_{DD} power supply should be larger than 5A, so that fuse built in the LCM could appropriately work under the abnormal condition.

Note 2: V_{CM}=+1.2V

The input terminal of LVDS transmitter is terminated with 100Ω.



Note 3: f_{CLK}=65.0MHz, and V_{DD}=3.3V, are the test conditions.



Note 4: For LVDS Transmitter Input

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	V_{LED}	Backlight Unit	10.8	12.0	13.2	V	Note 1
Enable	EN		4.5	5	5.5		-
Analog Dimming Function	ADIM		0	5	5.5		Note 2,3
Digital Dimming Function	DDIM	"H" Level	4.0	5	5.5		
		"L" Level	0	0	0.2		
LED Driving Current (DIM Control)	I_{LED}	ADIM = 0V, DDIM = 0% Duty	-	(1100)	-	mA	
		ADIM = 5V, DDIM = 100% Duty	-	(55)	-		
LED Lifetime	-	110mA x 3	-	(50k)	-	hrs	Note 4

Note 1: As Fig 5.1 shown, all LEDs are controlled by the LED Driver when applying 12V V_{LED}.

Note 2: Dimming function can be obtained by applying DC voltage or PWM signal from the display interface CN2. The recommend PWM signal is 1KHz~10KHz with 5V amplitude. The brightness is increased when applied DC voltage of ADIM or PWM duty of DDIM is decreased.

Note 3: 4A fuse is built in the LED voltage control board, current capacity for V_{LED} power supply should be larger than 10A, so that the fuse built in the LED voltage control board could appropriately work under the abnormal condition.

Note 4: The estimated lifetime is specified as the time to reduce 50% brightness by applying 110mA x 3 at 25°C.

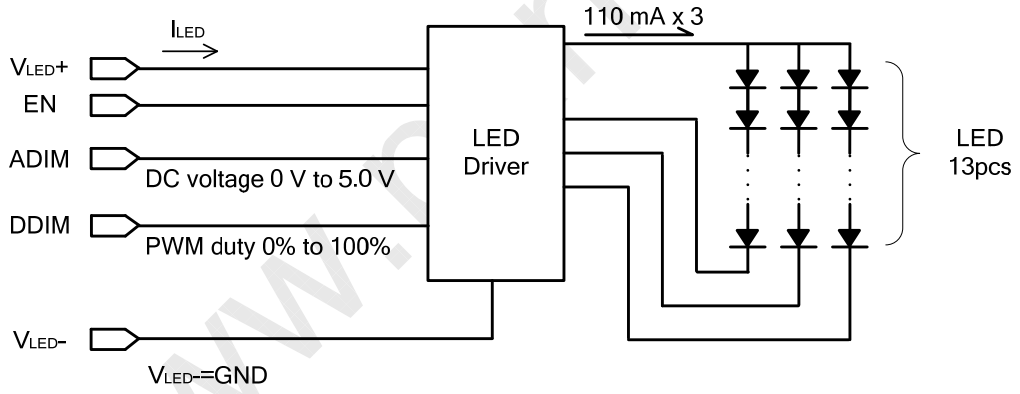
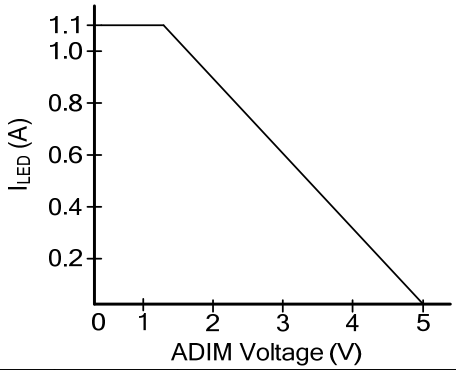


Fig 5.1

Note 5: I_{LED} vs DIM Voltage (Reference only)



6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The backlight unit needs to be turned on for 30 minutes.
- The ambient temperature is 25°C.
- In the dark room around 100~200 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C,\ V_{DD} = 3.3V$

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$, 110mA x 3	(960)	1200	-	cd/m^2	Note 1
Brightness Uniformity		-		(70)	80	-	%	Note 2
Contrast Ratio		CR		(450)	700	-	-	Note 3
Response Time (Rising + Falling)		$T_r + T_f$	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	25	35	ms	Note 4
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	(70)	80	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	(70)	80	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	(60)	70	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	(70)	80	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	(0.57)	0.62	(0.67)	-	Note 6
		Y		(0.30)	0.35	(0.40)		
	Green	X		(0.29)	0.34	(0.39)		
		Y		(0.55)	0.60	(0.65)		
	Blue	X		(0.10)	0.15	(0.20)		
		Y		(0.05)	0.10	(0.15)		
	White	X		(0.28)	0.33	(0.38)		
		Y		(0.30)	0.35	(0.40)		

Note 1: The brightness is measured from the panel center point, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \times 100\%$$

, which is based on the brightness values of the 5 points measured by BM-5 as shown in Fig. 6.2.

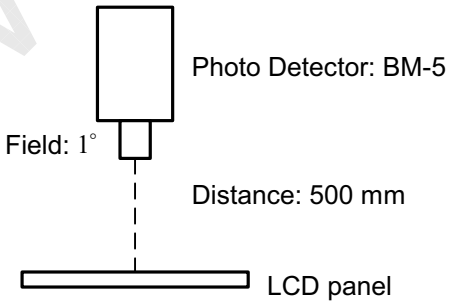


Fig. 6.1

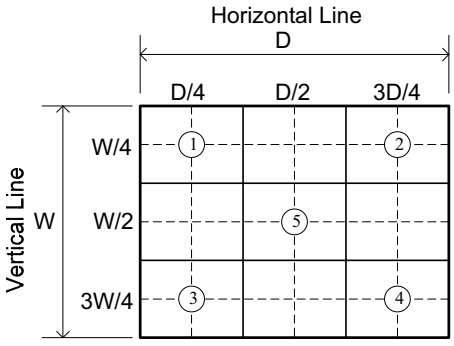


Fig. 6.2

Note 3: The Contrast Ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 90% brightness to 10% brightness when the data is from white to black. Oppositely, Falling time is the period from 10% brightness rising to 90% brightness.

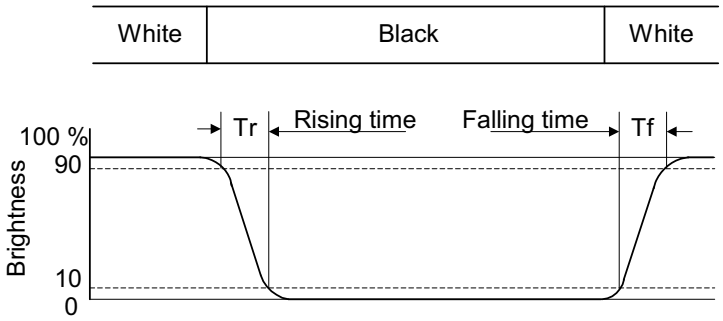


Fig . 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The viewing direction of this display is 12 o'clock, which means that a photograph with gray scale would not be reversed in color and the brightness change would be less from this direction. However, the best contrast peak would be located at 6 o'clock.

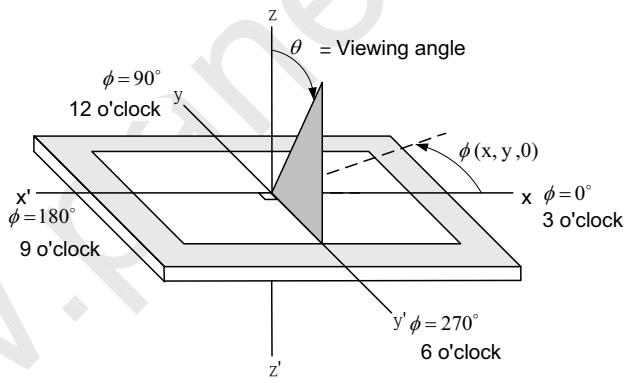
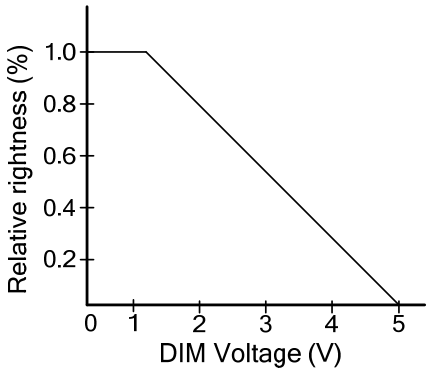


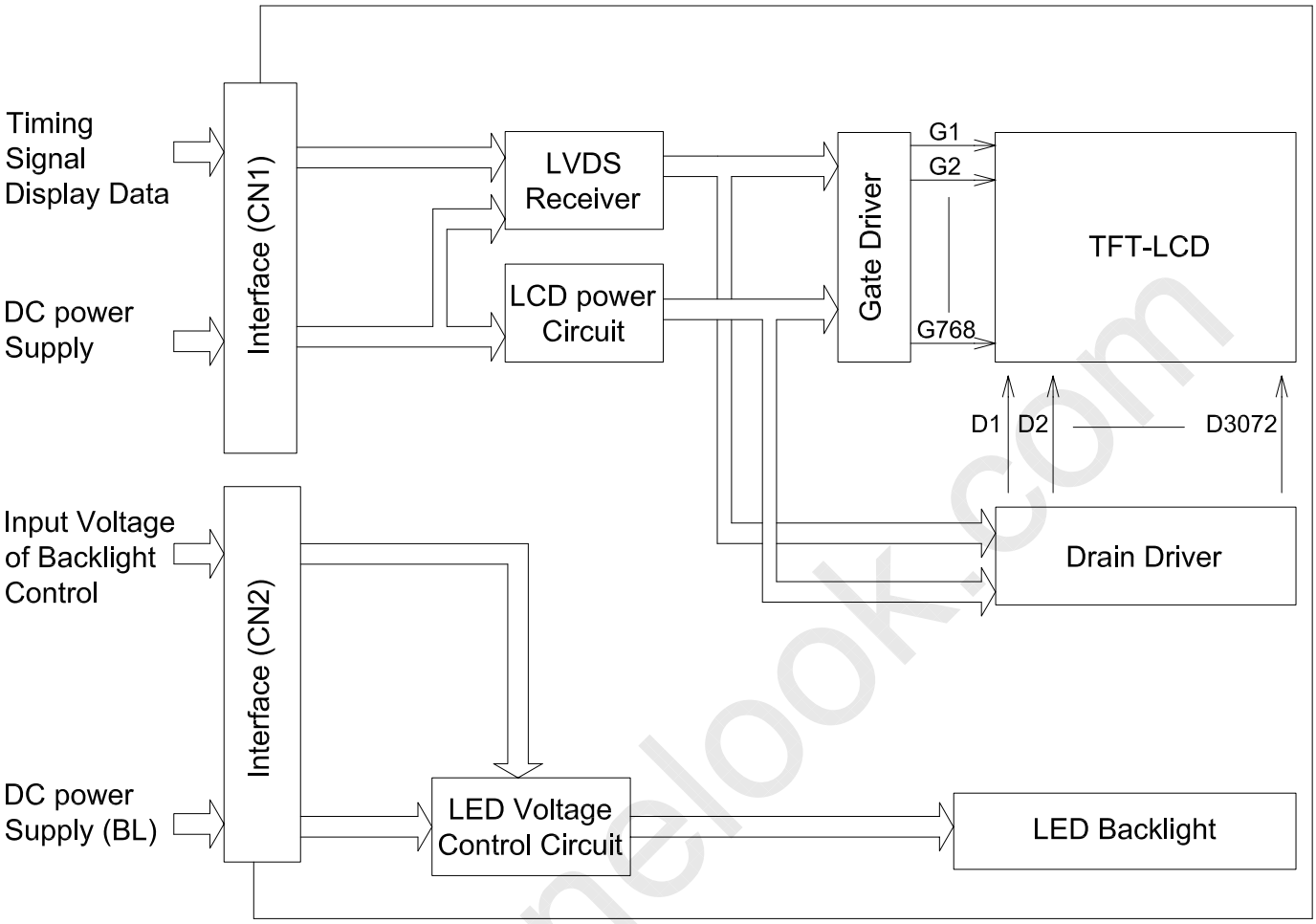
Fig 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

Note 7: Relative Brightness V.S DIM Voltage (Reference only)



7 BLOCK DIAGRAM



8. RELIABILITY TESTS

Test Item	Condition	
High Temperature	1) Operating 2) 80℃	240 hrs
Low Temperature	1) Operating 2) -30℃	240 hrs
High Temperature	1) Storage 2) 80℃	240 hrs
Low Temperature	1) Storage 2) -30℃	240 hrs
Thermal Shock	1) Non-Operating 2) -30℃ ↔ 80℃ 3) 0.5 hr ↔ 0.5 hr	240 hrs
High Temperature & Humidity	1) Operating 2) 40℃ & 85%RH 3) Without condensation (Note3)	240 hrs
Vibration	1) Non-Operating 2) 10～300 Hz 3) 1.5G 4) X, Y, and Z directions	10 min / cycle, 3cycles each direction
ESD	5) Operating 6) Tip: 150 pF, 330Ω,1 sec / cycle 7) Condition 1:Panel contact ± 8KV 8) Condition 2:Panel non-contact ± 15KV	-

Note 1: Display functionalities are inspected under the conditions defined in the specification after the reliability tests.

Note 2: The display is not guaranteed for use in corrosive gas environments.

Note 3: Under the condition of high temperature & humidity, if the temperature is higher than 40℃, the humidity needs to be reduced as Fig. 8.1 shown.

Note 4: Temperature of panel display surface area should be 80℃ Max.

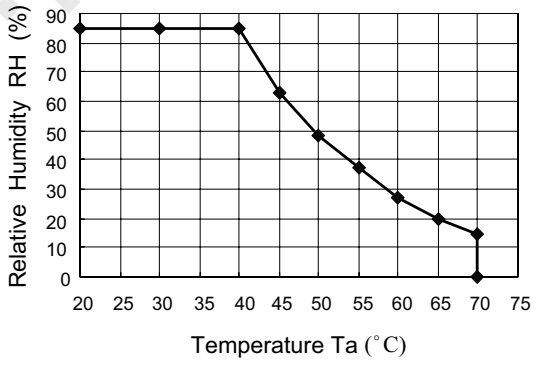


Fig. 8.1

9. LCD INTERFACE

9.1 INTERFACE PIN CONNECTIONS

The display interface connector is MSB240420G made by STM and more details of the connector are shown in the section of outline dimension.

Pin assignment of LCD interface is as below:

Pin No.	Signal	Function	Pin No.	Signal	Function
1	V_{DD}	Power Supply for Logic	11	IN2-	Pixel Data
2	V_{DD}		12	IN2+	
3	V_{SS}	GND	13	V_{SS}	GND
4	NC	No Connection	14	CLK IN-	Clock
5	IN0-	Pixel Data	15	CLK IN+	
6	IN0+		16	V_{SS}	GND
7	V_{SS}	GND	17	IN3-	Pixel Data
8	IN1-	Pixel Data	18	IN3+	
9	IN1+		19	V_{SS}	GND
10	V_{SS}	GND	20	FRC	High : 6 bit Mode (Note 2) Low or NC : 8 bit Mode (Note 2)

Note 1: IN n- and IN n+ (n=0,1,2,3),CLK IN- and CLK IN+ are recommended to be twisted or side-by-side FPC patterns, respectively.

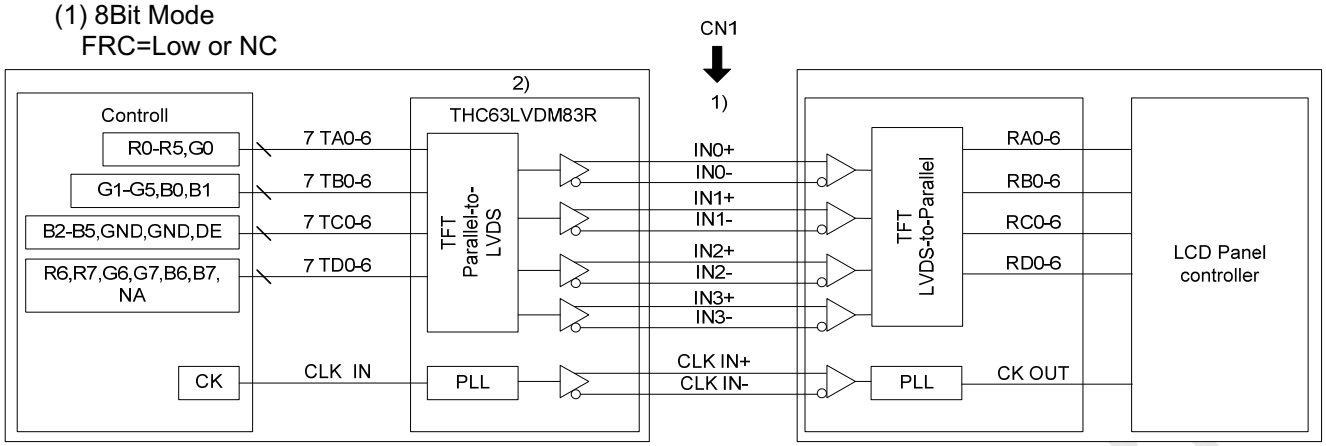
Note 2:"High" stands for 3.3V, "Low" stands for 0V and "NC" stands for no connection.

The backlight interface connector is SM08B-SRSS-TB made by JST, and pin assignment of backlight is as below:

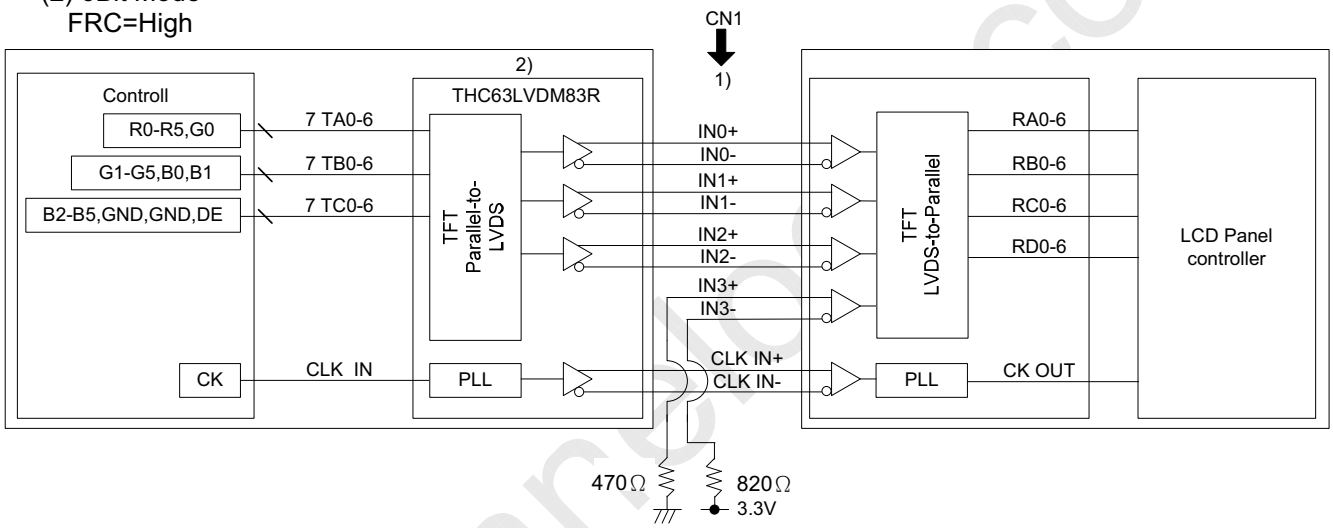
Pin No.	Signal	Level	Function
1,2	V_{LED+}	-	Power Supply for LED
3	NC	-	No Connection
4	EN	-	Enable Pin High : Backlight Enable Low : Backlight Disable
5	ADIM	-	Analog Voltage Dimming Function (Voltage Control)
6	DDIM	-	PWM Dimming Function
7,8	V_{LED-}	-	GND

9.2 LVDS INTERFALE

(1) 8Bit Mode
FRC=Low or NC



(2) 6Bit Mode
FRC=High



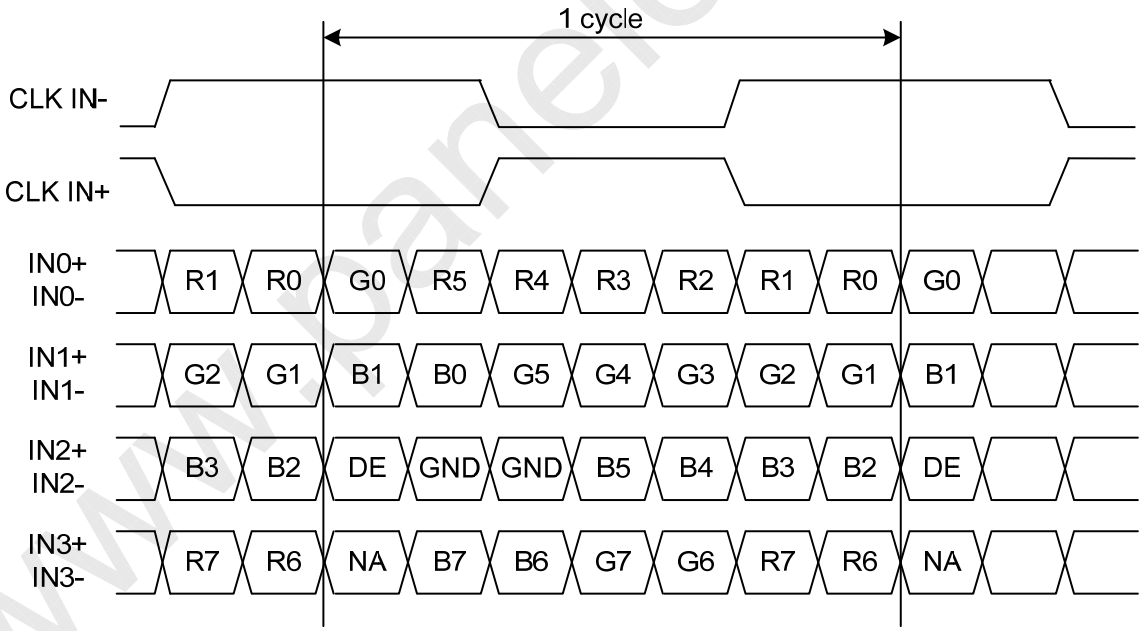
Note 1) LVDS cable impedance should be 100 ohms per signal line when each 2-lines(+,-) is used in differential mode.

Note 2) Transmitter Made by Thine : THC63LVDM83R equivalent.
Transmitter is not contained in Module.

9.3 LVDS DATA MAPPING

1) THC63LVDM83R Pin Assignment (8 Bit Mode)

Transmitter		FRC	Transmitter		FRC
Pin No.	Date	Low or NC	Pin No.	Date	Low or NC
51	TA0	R0 (LSB)	20	TC0	B2
52	TA1	R1	22	TC1	B3
54	TA2	R2	23	TC2	B4
55	TA3	R3	24	TC3	B5
56	TA4	R4	27	TC4	GND
3	TA5	R5	28	TC5	GND
4	TA6	G0 (LSB)	30	TC6	DE
6	TB0	G1	50	TD0	R6
7	TB1	G2	2	TD1	R7 (MSB)
11	TB2	G3	8	TD2	G6
12	TB3	G4	10	TD3	G7 (MSB)
14	TB4	G5	16	TD4	B6
15	TB5	B0 (LSB)	18	TD5	B7 (MSB)
19	TB6	B1	25	TD6	NA

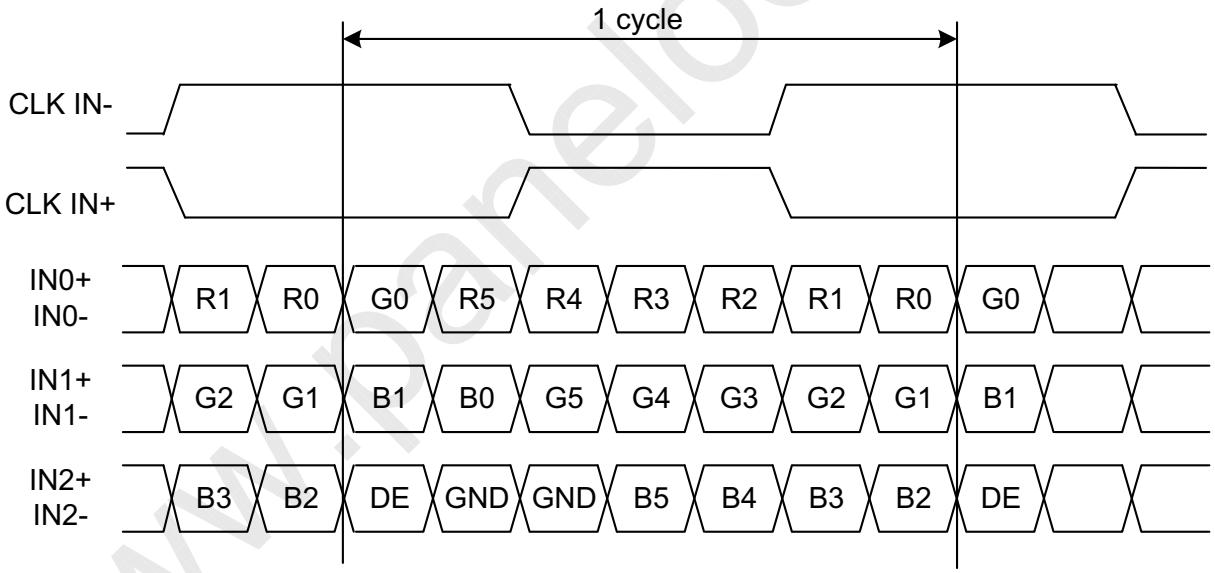


DE : Display Enable

NA : Not Available

2) THC63LVDM83R Pin Assignment (6 Bit Mode)

Transmitter		FRC	Transmitter		FRC
Pin No.	Date	High	Pin No.	Date	High
51	TA0	R0 (LSB)	20	TC0	B2
52	TA1	R1	22	TC1	B3
54	TA2	R2	23	TC2	B4
55	TA3	R3	24	TC3	B5 (MSB)
56	TA4	R4	27	TC4	GND
3	TA5	R5 (MSB)	28	TC5	GND
4	TA6	G0 (LSB)	30	TC6	DE
6	TB0	G1	50	TD0	NA
7	TB1	G2	2	TD1	NA
11	TB2	G3	8	TD2	NA
12	TB3	G4	10	TD3	NA
14	TB4	G5 (MSB)	16	TD4	NA
15	TB5	B0 (LSB)	18	TD5	NA
19	TB6	B1	25	TD6	NA



DE : Display Enable

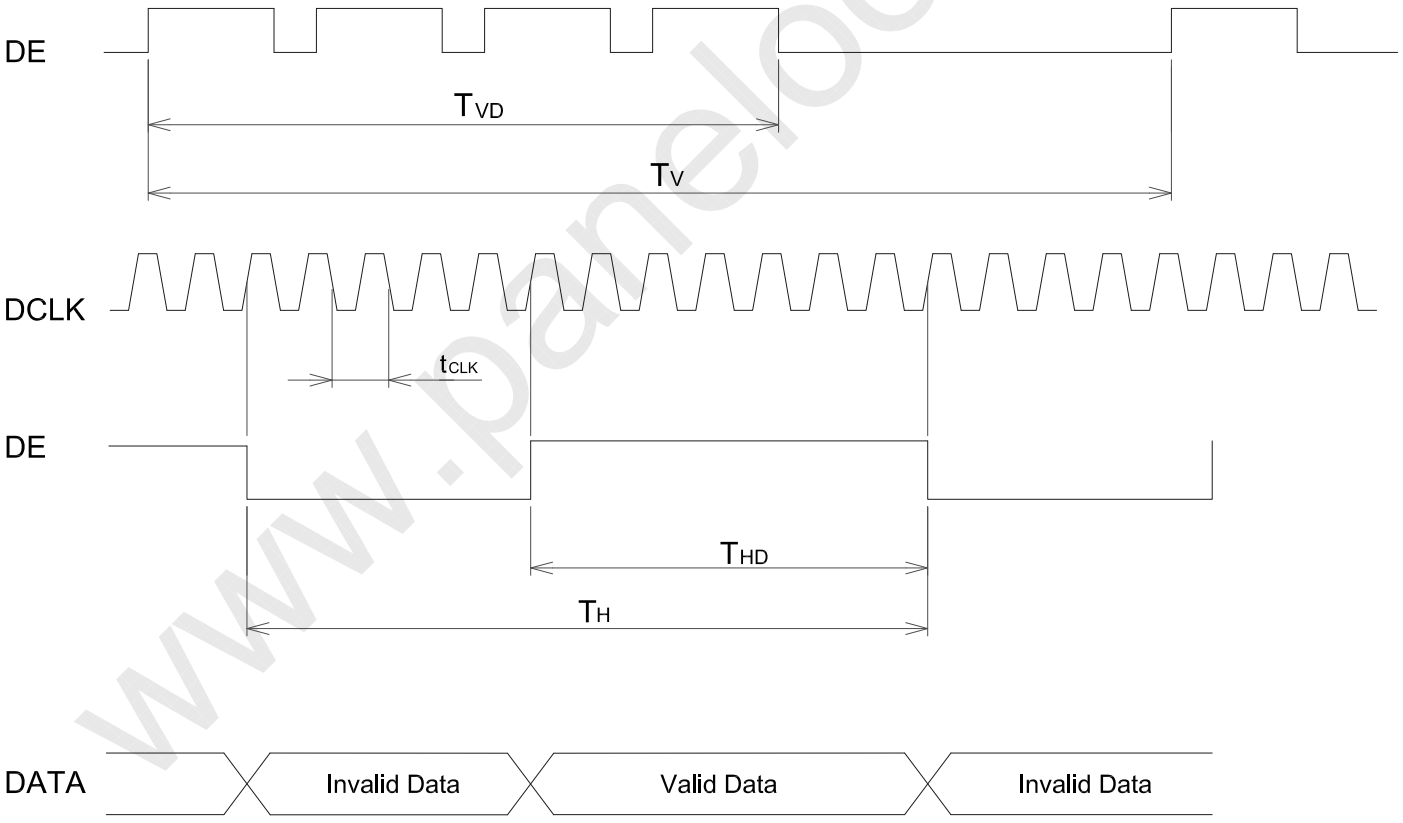
NA : Not Available.

8.4 INTERNAL TIMING SPECIFICATIONS

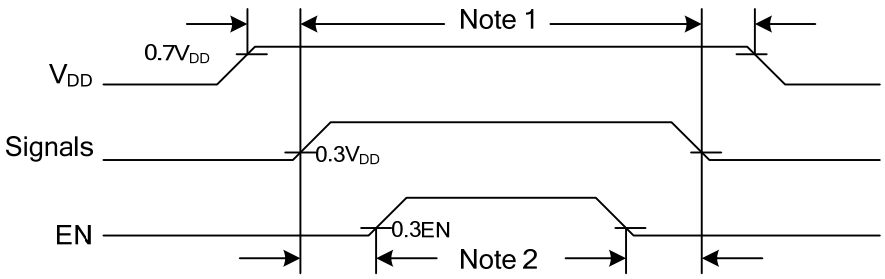
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
DCLK	Pixel Clock	1/t_{CLK}	-	65	80	MHz	-
DE	Vertical Total Time	T_V	780	806	1200	T_H	-
	Vertical Address Time	T_{VD}	768	768	768	T_H	-
	Horizontal Total Time	T_H	1140	1344	1600	t_{CLK}	-
	Horizontal Address Time	T_{HD}	1024	1024	1024	t_{CLK}	-

Note : The module is only operated by DE mode, Hsync and Vsync input signals should be set low logic level or ground . Otherwise, the module would operate abnormally.

8.5 INTERNAL TIMING DIAGRAM



9.6 POWER SEQUENCE



Power Sequence Timing

Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second. Hot plugging might cause display damage due to incorrect power sequence, please pay attention on interface connecting before power on.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

Note 3: The floating state of interface signal shonld be avoid at invalid period.

Note 4: When the interface signal is invalid, please set the power supply of V_{DD} to 0V.

9.7 DATA INPUT for DISPLAY COLOR(8 BIT MODE)

Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

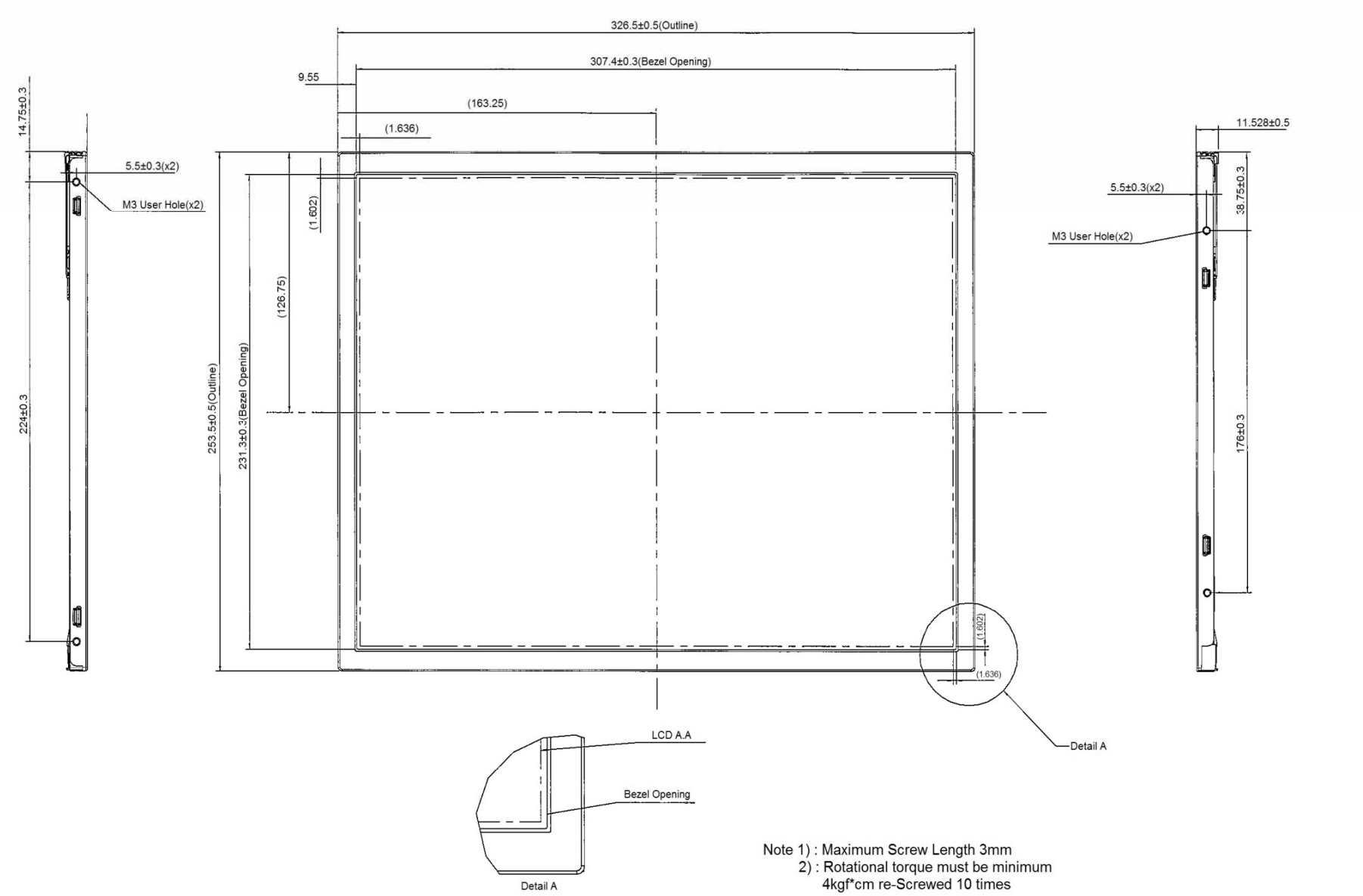
Note 2: Data Signal : 1 : High, 0 : Low

9.8 DATA INPUT for DISPLAY COLOR (6 BIT MODE)

	COLOR & Gray Scale	Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

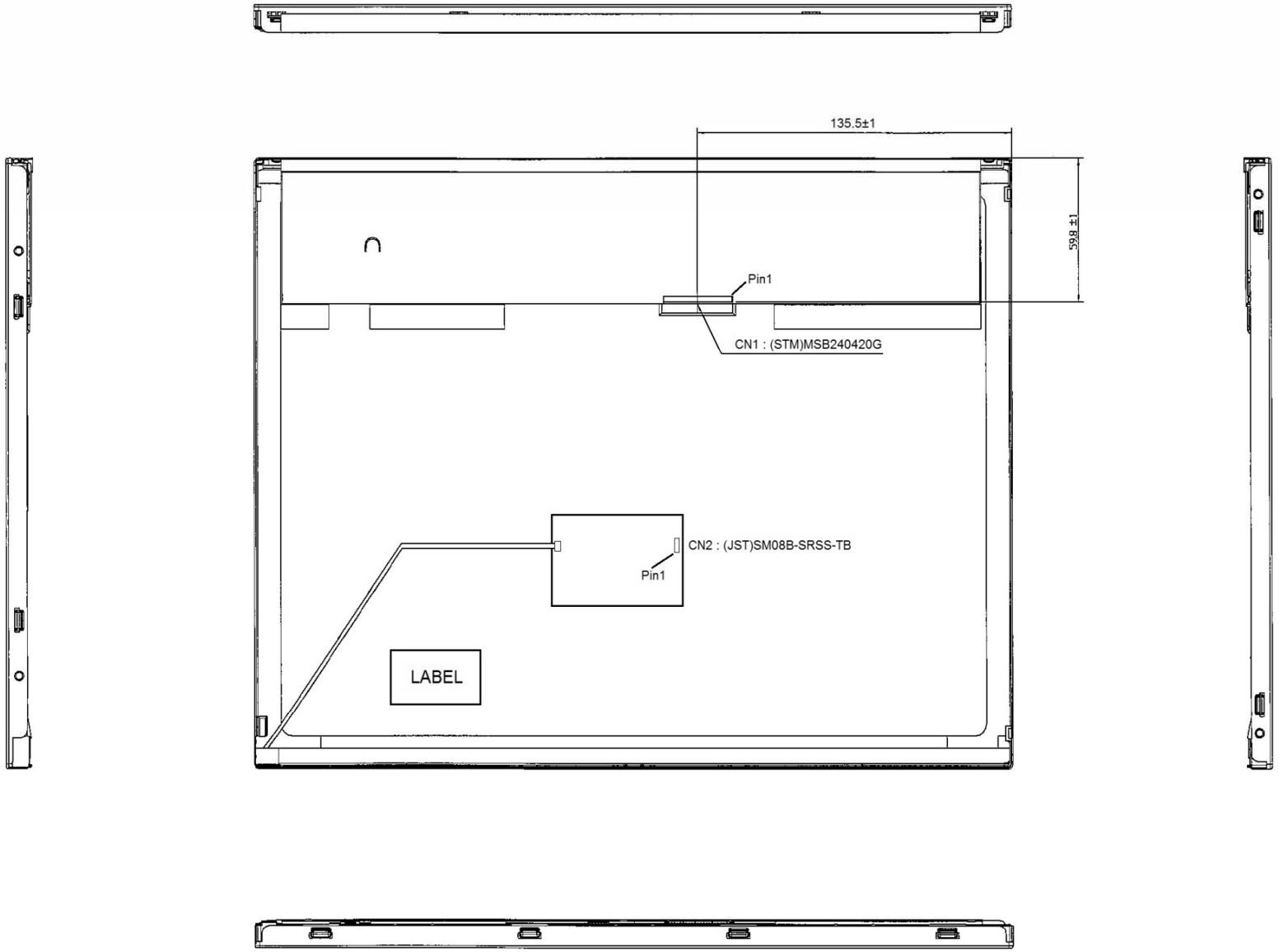
10. OUTLINE DIMENSIONS

10.1 FRONT VIEW



Note 1) : Maximum Screw Length 3mm
2) : Rotational torque must be minimum 4kgf*cm re-Screwed 10 times

9.2 FRAR VIEW



11. APPEARANCE STANDARD

The appearance inspection is performed based on the conditions as below:

- The distance between inspector's eyes and display is 35 cm.
- Ambient illumination:100~200 lx for light on inspection.
- The viewing angle to the front surface of display panel is 15 degree in vertical direction and 45 degree in horizontal direction.

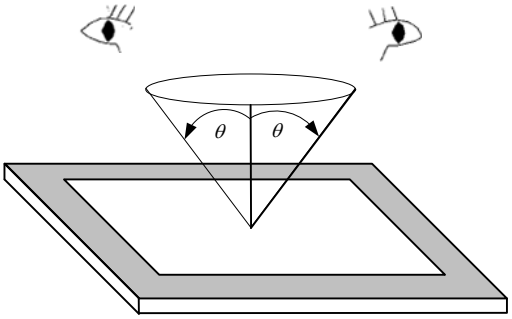


Fig. 10.1

11.1 THE DEFINITION OF LCD ZONE

LCD panel is divided into 3 areas as shown in Fig.10.2 for appearance specification in next section. A zone is the LCD active area (dot area); B zone is the area, which extended 1 mm out from LCD active area; C zone is the area between B zone and metal frame.

In terms of housing design, B zone is the recommended window area customers' housing should be located in.

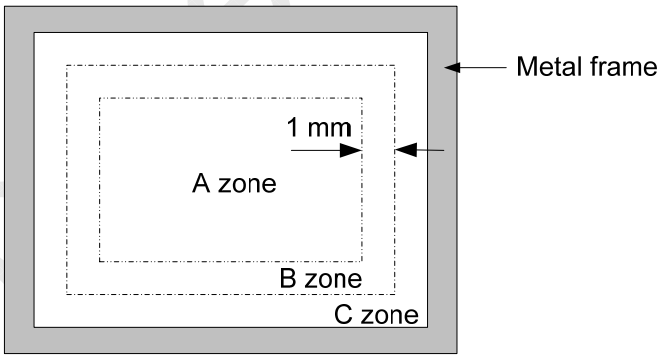


Fig. 10.2

11.2 LCD APPEARANCE SPECIFICATION

The specification as below is defined as the amount of unexpected phenomenon or material in a zone (LCD active area) panel. The definitions of length, width and average diameter using in the table are shown in Fig. 11.3.

Item	Criteria				Applied zone
Scratches on polarizer	Length (mm)	Width (mm)	Maximum number	Minimum space	A
	-	W≦0.05	Ignored	-	
	0.3＜L≦10	0.05＜W≦0.1	4	-	
Bubbles / Dent	Average diameter (mm)		Maximum number		A
	0.15＜D≦0.5		4		
1) Foreign Materials 2) Dark / White Spot	Filamentous (Line shape)				A
	Length (mm)	Width (mm)	Maximum number		
	-	W≦0.05	Ignored		
	0.3＜L≦2.0	0.05＜W≦0.1	4		
	Round (Dot shape)				A
	Average diameter (mm)		Maximum number		
	D≦0.15		Ignored		
	0.15≦D＜0.5		4		
Stain on polarizer	Those wiped out easily are acceptable				
Dot-Defect (Note 1)		Type	Maximum number		A
	Bright dot-defect	1 dot	3		
		2 adjacent dots	1		
		3 adjacent dots or above	Not allowed		
	Dark dot-defect	1 dot	5		
		2 adjacent dots	1		
		3 adjacent dots or above	Not allowed		
	In total		5		
	Minimum distance		10 mm		

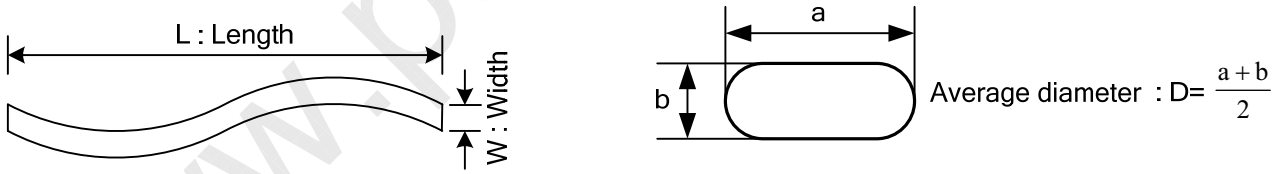


Fig 11.3

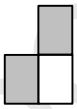
Note 1: The definitions of dot defect are as below:

- The defect area of the dot must be bigger than half of a dot.
- For bright dot-defect, the dot's appear bright and unchanged in size under showing black pattern.
- For dark dot-defect, the dot's appear dark and unchanged in size under pure red, green, blue and white pattern.
- The definition of 1-dot-defect is the defect-dot, which is isolated and no adjacent defect-dot.
- The definition of adjacent dot is shown as Fig. 11.5 to Fig 11.8.

2 dot adjacent
Fig. 11.5

2 dot adjacent
Fig. 11.6

2 dot adjacent (vertical)
Fig. 11.7



2 dot adjacent (slant)
Fig. 11.8

12. PRECAUTIONS

12.1 PRECAUTIONS of ESD

1) Before handling the display, please ensure your body has been connected to ground to avoid any damages by ESD. Also, do not touch display's interface directly when assembling.

2) Please remove the protection film very slowly before turning on the display to avoid generating ESD.

12.2 PRECAUTIONS of HANDLING

1) In order to keep the appearance of display in good condition, please do not rub any surfaces of the displays by using sharp tools harder than 3H, especially, metal frame and polarizer.

2) Please do not stack the displays as this may damage the surface. In order to avoid any injuries, please avoid touching the edge of the glass or metal frame and wore gloves during handling.

3) Touching the polarizer or terminal pins with bare hand should be avoided to prevent staining and poor electrical contact.

4) Do not use any harmful chemicals such as acetone, toluene, and isopropyl alcohol to clean display's surfaces.

5) Do not disassemble the module.

6) Please wipe any unknown liquids immediately such as saliva, water or dew on the display to avoid color fading or any permanent damages.

7) Do not have pressure or impulse on the module because the module will be damage.

8) Please use soft cloth without chemicals to clean the display by gently wiping.

12.3 PRECAUTIONS of OPERATING

1) Please input signals and voltages to the displays according to the values defined in the section of electrical characteristics to obtain the best performance. Any voltages over than absolute maximum rating will cause permanent damages to this display. Also, any timing of the signals out of this specification would cause unexpected performance.

2) When the display is operating at significant low temperature, the response time will be slower than it at 25℃.

3) The use of screen saver or sleep mode is recommended when static images are likely for long periods of time. This is to avoid the possibility of image sticking.

4) Spike noise can cause malfunction of the circuit. The recommended limitation of spike noise is no bigger than 100 mV p-p.

5) Moisture come into or contact the LCD module may damage LCD module when it is operating.

6) The LED driver board with cable can't be pulled strongly or cable connector will be damaged.

12.4 PRECAUTIONS of STORAGE

If the displays are going to be stored for years, please be aware the following notices.

1) Please store the displays in a dark room to avoid any damages from sunlight and other sources of UV light.

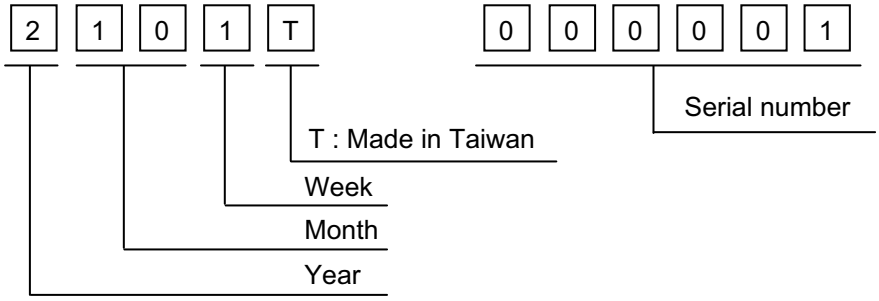
2) Please store LCD module within the specified storage conditions.

3) It would be better to keep the displays in the container, which is shipped from KOE, and do not unpack it.

4) Please do not stick any labels on the display surface for a long time, especially on the polarizer.

13. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.13.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.



2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Mark
2012	2
2013	3
2014	4
2015	5
2016	6

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

Week (Days)	Mark
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

3) Except letters I and O, revision number will be shown on lot mark and following letters A to Z.

4) The location of the lot mark is on the back of the display shown in Fig. 13.1.

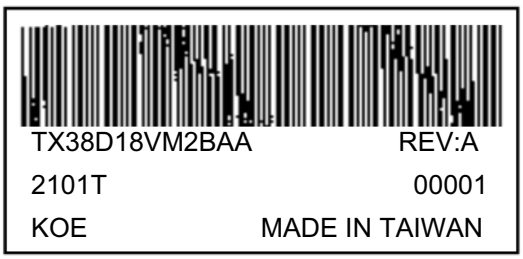


Fig. 13.1